CLAIMS

1. A scan flip-flop circuit comprising:

a usual mode data input terminal;

a scan-in data input terminal;

an output terminal;

a first master latch circuit, connected between said usual data input terminal, for receiving usual mode data at said usual data input terminal in synchronization with a first clock signal;

a second master latch circuit, connected to said scan-in data input terminal and said output terminal, for receiving scan-in data at said scan-in data input terminal in synchronization with first and second scan clock signals; and

a slave latch circuit, connected between said first master latch circuit and said output terminal, for receiving an output signal of said first master latch circuit in synchronization with said first clock signal and said second scan clock signal,

said slave latch circuit comprising a control circuit, connected between an output of said first master latch circuit and said output terminal, for controlling transfer of said usual mode data to said output terminal in synchronization with a second clock signal independent of said first clock signal.

2, The scan flip-flop circuit as set forth in claim 1, wherein said second clock signal is said second scan clock signal.

3. The scan flip-flop circuit as set forth in claim 1, wherein said first master latch circuit comprises:

a first transfer gate connected to said usual mode data input terminal;

a first inverter connected to said first transfer gate;

a second transfer gate connected between said

first inverter and said slave latch circuit; and

a second inverter and a third transfer gate connected in series between an input and an output of said first inverter,

said first, second and third transfer gates being controlled in synchronization with said first clock signal, so that said first transfer gate is operated opposite to said second and third transfer gates.

4. The scan flip-flop circuit as set forth in claim 1, wherein said slave latch circuit comprises:

a third inverter connected between said first master latch circuit and said control circuit, said control circuit being connected to said output terminal; and

a fourth inverter and a fourth transfer gate connected in series between said output terminal and the output of said first master latch circuit,

said fourth transfer gate being controlled in synchronization with said first clock signal.

5. The scan flip-flop circuit as set forth in claim 1, wherein said second master latch circuit comprises:

first and sixth transfer gates connected between said scan-in data input terminal and said output terminal; and

fifth and sixth inverters and a seventh transfer gate connected in series to a connection between said fifth and sixth inverters,

said first and seventh transfer gates being controlled in synchronization with said first scan clock signal, so that said fifth transfer gate is operated opposite to said seventh transfer gate,

said sixth transfer gate being controlled in synchronization with said second scan clock signal.

6. The scan flip-flop circuit as set forth in claim 1, wherein said first master latch circuit comprises:

a first transfer gate connected to said usual

mode data input terminal;

a first NOR gate having a first input connected to said first transfer gate and a second input for receiving a set signal;

a second transfer gate connected between said first NOR gate and said slave latch circuit; and

a first inverter and a third transfer gate connected in series between the first input and an output of said first NOR gate,

said first, second and third transfer gates being controlled in synchronization with said first clock signal, so that said first transfer gate is operated opposite to said second and third transfer gates.

7. The scan flip-flop circuit as set forth in claim 1, wherein said slave latch circuit comprises:

a second inverter connected between said first master latch circuit and said control circuit, said control circuit being connected to said output terminal; and

a second NOR gate having a first input connected to said second inverter, a second input for receiving a set signal, and an output;

a fourth transfer gate connected between the output of second NOR gate and the output of said first master latch circuit,

said fourth transfer gate being controlled in synchronization with said first clock signal.

8. A scan flip-flop circuit comprising:

a usual mode data input terminal;

a scan-in data input terminal;

an output terminal;

a first master latch circuit, connected to said usual data input terminal, for receiving usual mode data at said usual data input terminal in synchronization with a clock signal;

a second master latch circuit, connected to

said scan-in data input terminal and said output terminal, for receiving scan-in data at said scan-in data input terminal in synchronization with first and second scan clock signals;

a slave latch circuit, connected between said first master latch circuit and said output terminal, for receiving an output signal of said first master latch circuit in synchronization with said clock signal and said second scan clock signal,

said slave latch circuit comprising a control circuit, connected between an output of said first master latch circuit and said output terminal, for controlling transfer of said usual mode data to said output terminal in synchronization with said second scan clock signal, so that when said second master latch circuit generates an output signal and transmits it to said output terminal, said control circuit stops transfer of said usual mode data to said output terminal.